TPS22933 Triple-Input Power Multiplexer With Auto-Select and Low Drop-Out Voltage Regulator

1 Features

- Three Integrated Load Switches Automatically Choose Highest Input
- Integrated 3.6-V Fixed LDO
- Switched and Always on LDO Outputs
- µQFN package 1.5 mm × 1.5 mm
- Input Voltage Range: 2.5 V to 12 V
- Low ON-Resistance (r_{ON})
  – r_{ON} = 2.4 Ω at V_{IN} = 5.0 V
  – r_{ON} = 2.6 Ω at V_{IN} = 4.2 V
- 50-mA Maximum Continuous Current
- Low Threshold Control Input (EN)
- Switchover Time of 18 µs (typical)

2 Applications

- Smart Phones
- GPS Devices
- Digital Cameras
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Portable Instrumentation

3 Description

The TPS22933 device is a small, low r_{ON}, triple-input power multiplexer with auto-input selection and a low-dropout linear regulator. The device contains three P-channel MOSFETs that can operate over an input voltage range of 2.5 V to 12 V. The TPS22933 automatically selects the highest level (from BAT, USB, and DC_IN) and enables that input to source the LDO. LOUT is an always-on output from the LDO. The Enable function (EN pin) allows VOUT to be switched on or off, enables a quick discharge resistor, and is capable of interfacing directly with low-voltage control signals.

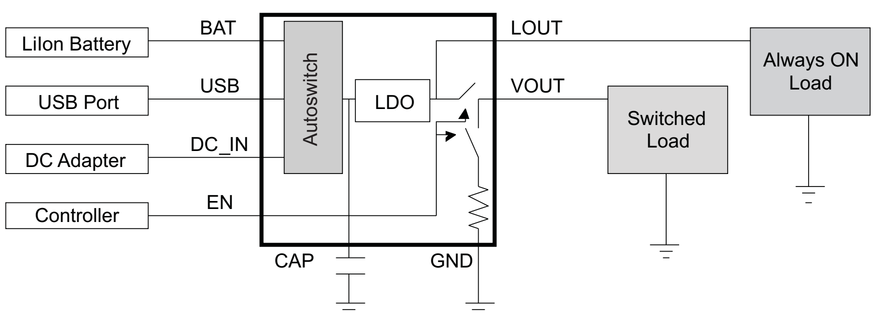
The TPS22933 is available in a small, space-saving 8-pin µQFN package and is characterized for operation over the free-air temperature range of –40ºC to 85ºC.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22933	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2011) to Revision A	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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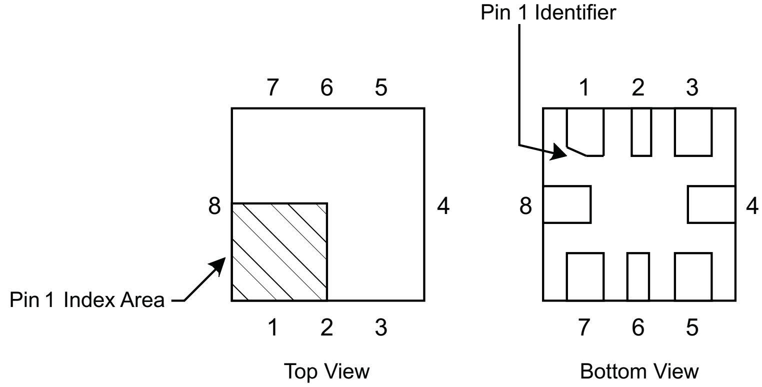
5 Pin Configuration and Functions

RSE Package
8-PIN UQFN



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BAT	I	Source Voltage 1 (Battery)
2	USB	I	Source Voltage 2 (V+ USB)
3	DC_IN	I	Source Voltage 3 (DC Adapter)
4	GND	—	Ground
5	EN	I	VOUT Enable (Cannot be left floating)
6	CAP	O	Capacitor for LDO
7	VOUT	O	Switched LDO Output
8	LOUT	O	Always on LDO Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VIN	Input voltage	BAT, USB, DC_IN	–0.3	14	V
VOUTPUT	Output voltage	VOUT, LOUT	–0.3	6	V
VEN	Input voltage	EN	–0.3	6	V
IMAX	Maximum continuous switch current			75	mA
IPLS	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle			100	mA
T_A	Operating free-air temperature		–40	85	°C
T_{lead}	Maximum lead temperature (10-s soldering time)			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	BAT, USB, DC_IN	2.5		12	V
V_{EN}		EN	0		5.5	V
V_{IH}	EN pin High-level input voltage, (EN > V_{IH} Min, VOUT = LDO Output)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	1.15		5.5	V
V_{IL}	EN pin Low-level input voltage, (EN< V_{IL} Max, VOUT = pulldown)	BAT = 2.5 V to 5.5 V, USB, DC_IN = 2.5 V to 12 V	0		0.6	V
$I_{OUT\text{-}LOUT}$	LOUT Current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V, $I_{OUT\text{-}VOUT}$ = 0 mA			50	mA
$I_{OUT\text{-}VOUT}$	VOUT Current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V, $I_{OUT\text{-}LOUT}$ = 0 mA			50	mA
$I_{OUT\text{-}TOTAL}$	LOUT + VOUT current	V_{BAT} = 4.2 V OR V_{USB} = 5 V OR V_{DC_IN} = 5 V, EN = 3.4 V			50	mA
CAP	LDO Capacitor (on CAP pin)		20[1]			nF
	LOUT Capacitor			1		µF
	VOUT Capacitor			1		µF

(1) Refer to *Application and Implementation*.

6.4 Thermal Information

THERMAL METRIC[1]		TPS22933 RSE (UQFN) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

BAT = 2.5 V to 12.0 V, USB = 2.5 V to 12.0 V, DC_IN = 2.5 V to 12.0 V, T_A = –40ºC to +85ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1) (2) (3)	T_A	MIN	TYP(4)	MAX	UNIT
$I_{IN\text{-}BAT}$	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 3 V, V_{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 3 V, EN = 3.4 V			0.7	2	
$I_{IN\text{-}USB}$	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 3 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2V, V_{USB} = 5V, V_{DC_IN} = 5.5V, EN = 3.4 V			0.7	2	
$I_{IN\text{-}DC\_IN}$	Operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 3 V, V_{DC_IN} = 5 V, EN = 3.4 V	Full		9.2	15	µA
	Quiescent current	I_{OUT} = 0, V_{BAT} = 4.2V, V_{USB} = 5.5V, V_{DC_IN} = 5V, EN = 3.4 V			0.7	2	
$I_{IN\text{-}USB}$	Hi-Voltage operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 12 V, V_{DC_IN} = 5 V, EN = 3.4 V	Full		10.8	20	µA
$I_{IN\text{-}DC\_IN}$	Hi-Voltage operating current	I_{OUT} = 0 mA, V_{BAT} = 4.2 V, V_{USB} = 5 V, V_{DC_IN} = 12 V, EN = 3.4 V	Full		10.8	20	µA
R_{ON}	ON resistance (USB to CAP, BAT to CAP, DC_IN to CAP)	V_{IN} = 5.0 V, I_{OUT} = 10 mA	25ºC		2.4	3.3	Ω
			Full			3.5	
		V_{IN} = 4.2 V, I_{OUT} = 10 mA	25ºC		2.6	3.5	Ω
			Full			4	
		V_{IN} = 2.5 V, I_{OUT} = 10 mA	25ºC		3.8	5	Ω
			Full			6	
R_{ONVOUT}	ON resistance (LDO output to VOUT)	V_{IN} = 4.2 V, $I_{OUT\text{-}VOUT}$ = 10 mA	25ºC		1.3	2.5	Ω
			Full			3	
R_{PD}	Output pulldown resistance	V_{IN} = 4.2 V, V_{EN} = 0 V, I(into VOUT) = 10 mA	25ºC		63.8	120	Ω
I_{EN}	EN input leakage	V_{EN} = 1.6 V to 5.5 V or GND	Full			1	µA
$V_{DO\text{-}VOUT}$	Dropout voltage VOUT (5) (6)	I_{OUT} = 10 mA	Full		0.11		V
$V_{DO\text{-}LOUT}$	Dropout voltage LOUT	I_{OUT} = 10 mA(5) (6)	Full		0.1		V
V_{LOUT}	Always on LDO output voltage (LOUT pin)	V_{IN} < 3.4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full		$V_{IN} - V_{DO\text{-}LOUT}$		V
		V_{IN} > 4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full	3.42	3.6	3.78	
V_{VOUT}	Switched LDO output voltage (VOUT pin)	V_{IN} < 3.4 V, I_{OUT} = 10 m A, V_{EN} = 1.8 V	Full		$V_{IN} - V_{DO\text{-}VOUT}$		V
		V_{IN} > 4 V, I_{OUT} = 10 mA, V_{EN} = 1.8 V	Full	3.39	3.57	3.75	
V_{CO}	Changeover voltage	V_{BAT} = 4.2 V, V_{USB} = 4.0 V rising to 4.4 V	Full		0.15		V
t_{CO}	Changeover time	VBAT=4.2 V, V_{USB} = 4.0 V rising to 4.4 V, CAP = 0.01 µF, I_{OUT} = 10 mA	25ºC		18		µs
			Full			50	
t_{OFF}	VOUT OFF-time	EN high to low, C(VOUT) = 1 µF, VOUT load = 360 Ω	Full		32		µs
t_{ON}	VOUT ON-time	EN low to high, C(VOUT) = open, VOUT load = 360 Ω	Full		65		µs

(1) V_{IN} is defined as the highest voltage present on the BAT, USB and DC_IN pins.
(2) One of the voltages on BAT, USB and DC_IN must be > VIN (Min), others can be 0 V.
(3) V_{BAT}, V_{USB} and V_{DC_IN} refer to the voltages on BAT, USB and DC_IN respectively. OUT, IOUT-VOUT and IOUT-LOUT refer to the currents for the combined output current for VOUT and LOUT, the current on VOUT and the current on LOUT respectively.
(4) TYP is 25ºC, BAT = 4.2-V, USB = 0-V, DC_IN = 0-V.
(5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} - V_{DROPOUT}$.
(6) Dropout voltage is measured at the VIN that causes the output to drop to 100mV below its nominal voltage. For VOUT, the voltage drop across the output switch is included (10mA × R_{ONVOUT}).

6.6 Typical Characteristics

Table 1. Performance Graphs and Plots

Type	Description	Figure
Graph	RON versus VIN (BAT, USB, DC_IN) 25°C	Figure 1
Graph	RON versus VIN (Any input)	Figure 2
Graph	Quiescent Current versus Input Voltage (Any input)	Figure 3
Graph	Operating Current versus Input Voltage (Any Input)	Figure 4
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 5
Scope Plot	t_{OFF} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 6
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = 1 uF, 25°C)	Figure 7
Scope Plot	t_{ON} (VIN = 4.2 V, C(VOUT) = open, 25°C)	Figure 8
Graph	LOUT and VOUT versus Temperature at VIN = 4.2 V	Figure 9
Graph	LOUT and VOUT versus IOUT (VIN = 4.2 V, Temp = 25°C)	Figure 10
Graph	LOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 11
Graph	VOUT Dropout Voltage versus Temperature (VIN = 2.5 V)	Figure 12
Graph	Output Pulldown Resistance (R_{PD}) versus Temperature (10 mA into VOUT)	Figure 13

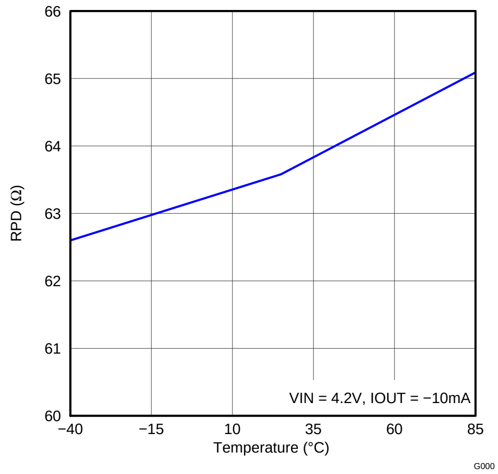


Figure 1. RPD vs Temperature

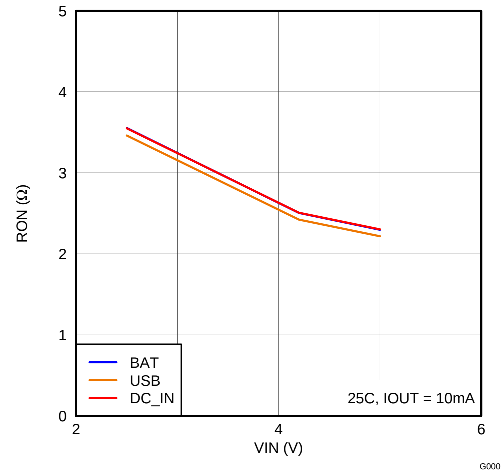


Figure 2. R_{ON} vs VIN (Typical)

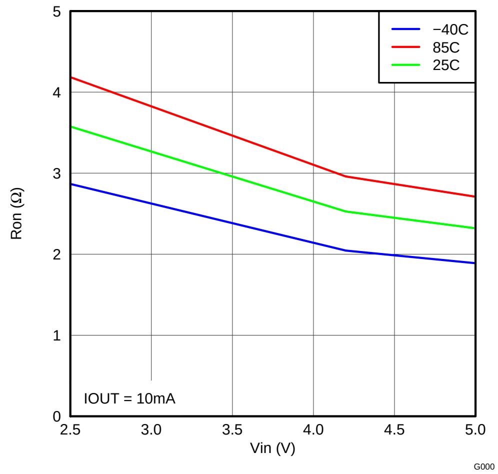


Figure 3. R_{ON} vs VIN

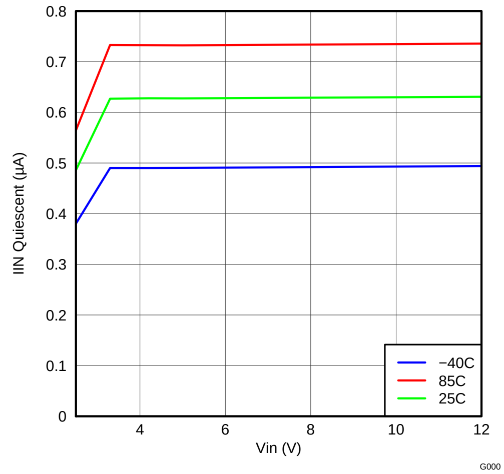


Figure 4. I_{IN} (Quiescent) vs VIN

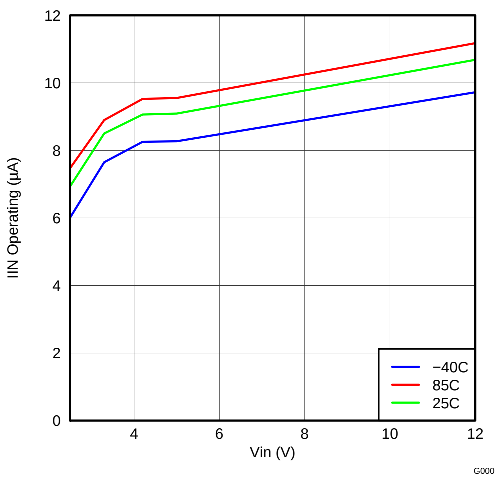


Figure 5. I_{IN} (Operating) vs VIN

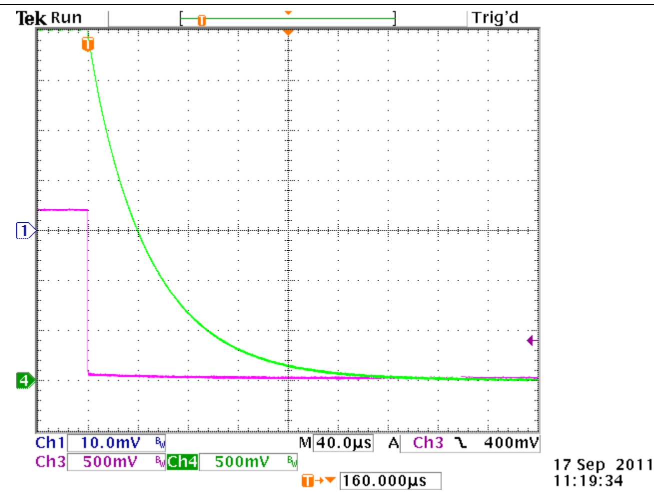


Figure 6. VOUT t_{OFF} (1 µF on VOUT)

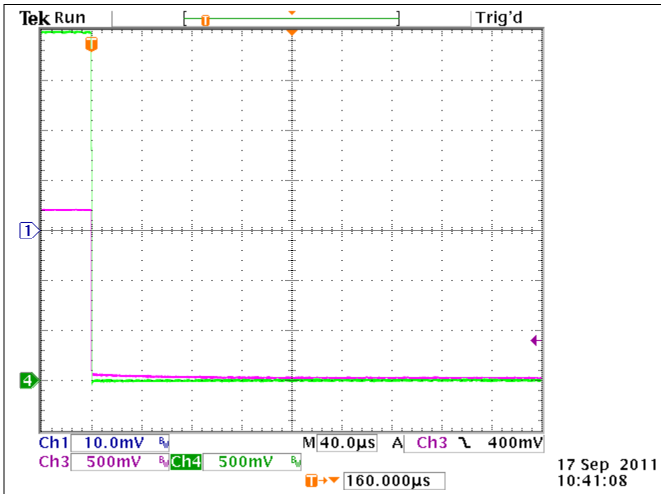


Figure 7. VOUT t_{OFF} (No Capacitor on VOUT)

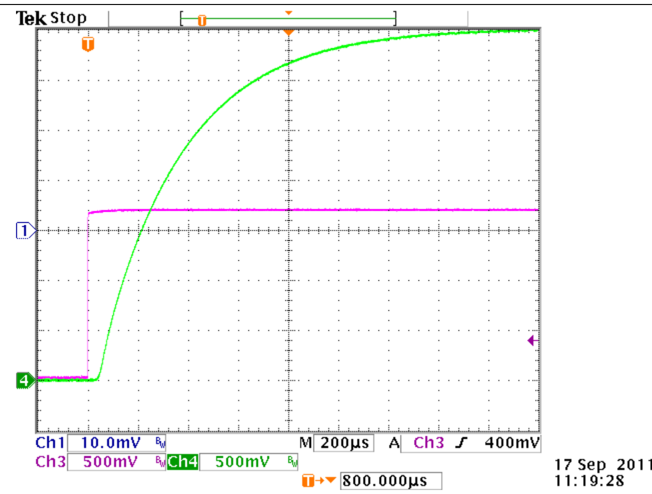


Figure 8. VOUT t_{ON} (1 µF on VOUT)

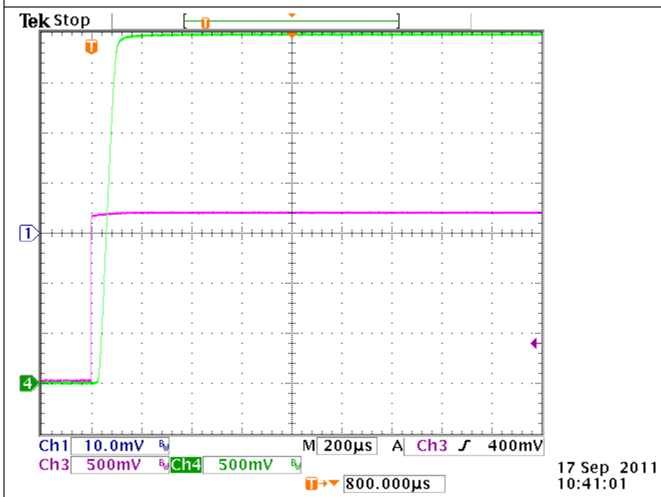


Figure 9. VOUT t_{ON} (No Capacitor on VOUT)

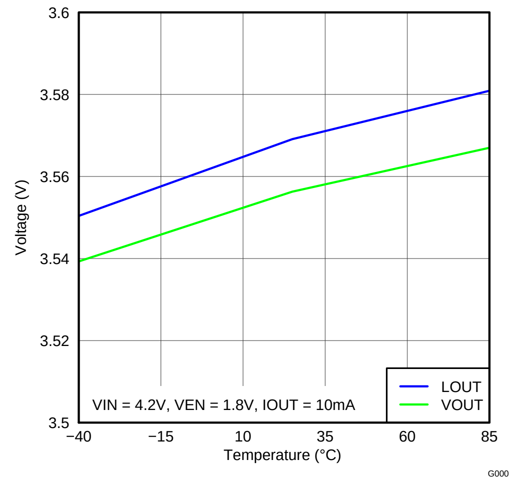


Figure 10. LOUT-VOUT vs Temperature VIN 4.2 V

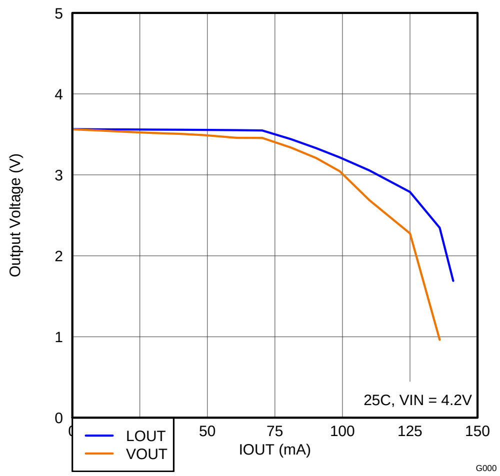


Figure 11. LOUT-VOUT vs IOUT

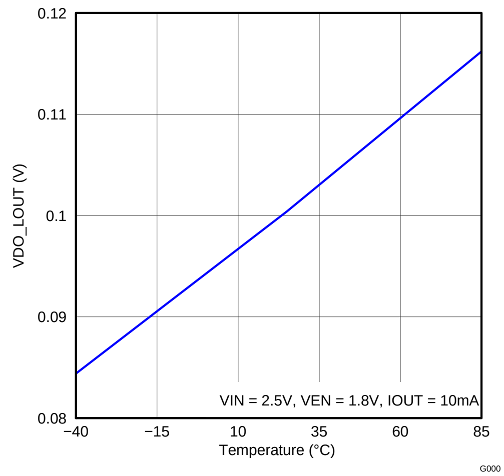


Figure 12. VDOLOUT vs Temperature VIN 2.5 V

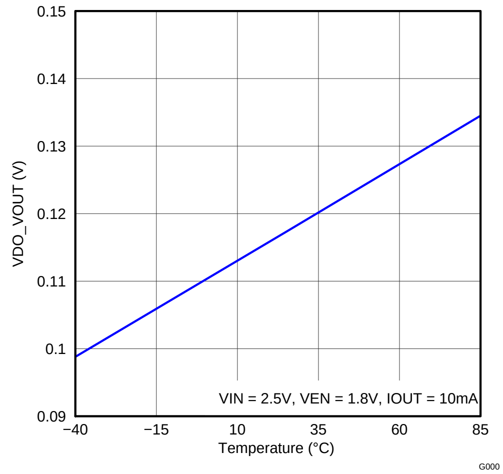


Figure 13. VDOVOUT vs Temperature VIN 2.5 V

7 Parametric Measurement Information

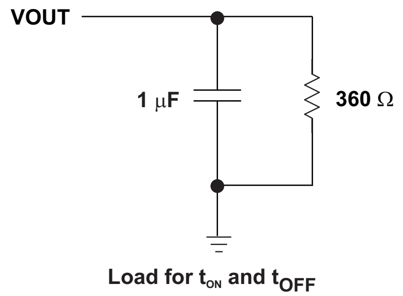


Figure 14. Test Circuit and t_{ON} / t_{OFF} Waveforms

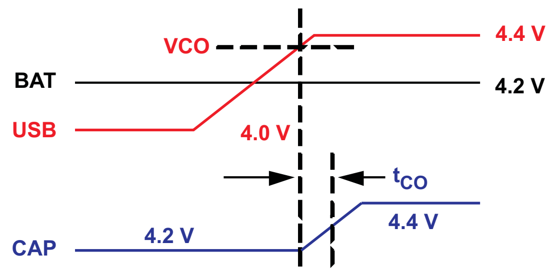


Figure 15. Switchover Timing

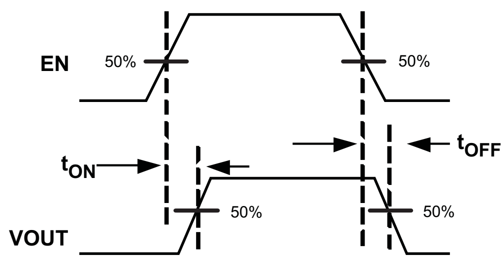


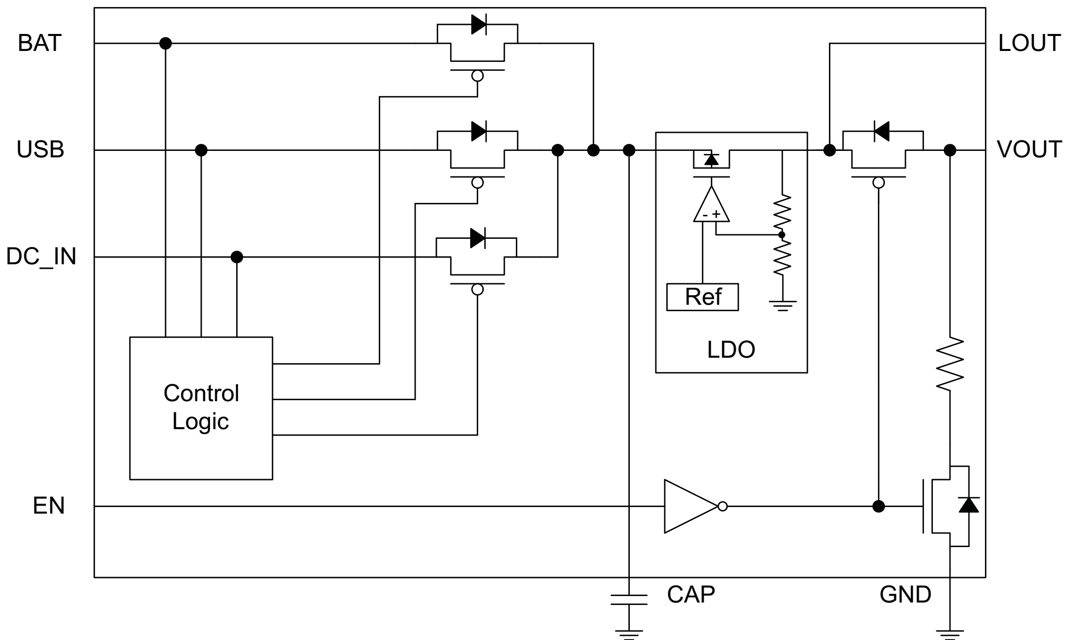
Figure 16. VOUT Enable Timing

8 Detailed Description

8.1 Overview

The TPS22933 is a triple-input power multiplexer with auto-input selection and a low dropout linear regulator. The device contains three P-channel MOSFETs that can operate over an input voltage range of 2.5 V to 12 V. The TPS22933 automatically selects the highest voltage level (from BAT, USB, and DC_IN) and enables that input to source the LDO. LOUT is an always-on output from the LDO, but VOUT can be switched on and off using the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The EN pin controls the state of the VOUT switch and VOUT pulldown switch. EN has no control over LOUT. Asserting EN enables the VOUT switch and disables the Quick Output Discharge (QOD) switch. Deasserting EN disables the VOUT switch and enables the QOD switch. EN is active high and has a low threshold, making it capable of interfacing with low voltage signals. The EN pin is compatible with standard GPIO Logic threshold and can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V or 3.3-V GPIOs.

8.3.2 Power Changeover

The TPS22933 LDO is powered by the highest level input. When input voltages change, the TPS22933 may change which input powers the LDO. During initial power up, the input that reaches the highest value first will power the LDO. Once that decision is made, changing between input sources is based on VCO. When an input source becomes VCO over the input currently supplying power to the LDO, changeover will occur and the new, higher input will power the LDO.

8.4 Device Functional Modes

Table 2 and Table 3 show the behavior of the device with various voltage conditions for the inputs and enable pin.

Table 2. Function Table

EN	LDO TO LOUT	LDO TO VOUT	VOUT TO GND
L	ON	OFF	ON
H	ON	ON	OFF

Table 3. Input Selection Table (V1 > V2 > V3)

BAT	USB	DC_IN	LDO SUPPLY
V1	V2 or V3	V2 or V3	BAT
V2 or V3	V1	V2 or V3	USB
V2 or V3	V2 or V3	V1	DC_IN
V1	V1	V1	See (1)

(1) Whichever source achieves the highest level the fastest will supply the LDO.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 LDO Capacitor (for CAP Pin)

An optional capacitor on the CAP pin helps stabilize the integrated LDO. Take care in capacitor sizing to reduce inrush currents. The voltage on the CAP pin will follow the highest input. Since the max input voltage is 12 V, the capacitor voltage rating must be higher than 12 V.

9.1.2 Using the CAP Pin as a Power Output

Figure 17 shows three power inputs multiplexed to source only through the CAP pin. In this case, the LDO outputs are not used (EN is tied low). The highest of the inputs is chosen to drive the voltage at the CAP pin.

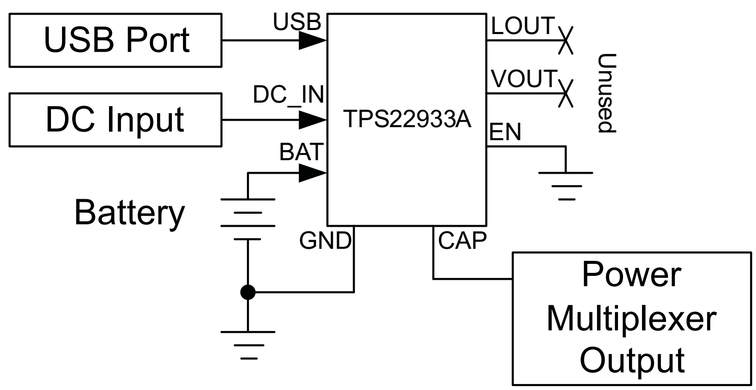


Figure 17. Using the CAP Pin as a Multiplexer Output

9.2 Typical Application

Figure 18 shows three power inputs multiplexed to source the LDO. The LDO always on output (LOUT) is tied to an MSP430. The MSP430 then determines when to enable the switched output (VOUT) by driving the EN pin.

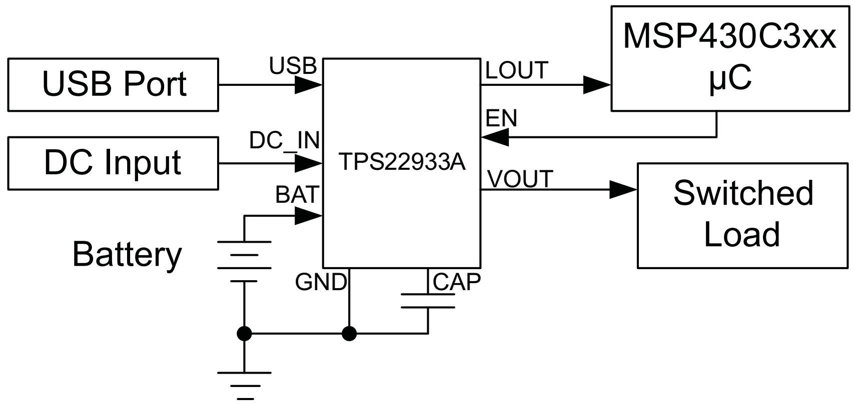


Figure 18. Application Example

Typical Application (continued)

9.2.1 Design Requirements

Table 4 lists the design parameters for TPS22933.

Table 4. Design Parameters

INPUT	VOLTAGE
USB Port	5.0V
DC Input	5.0V
Battery	4.2V

9.2.2 Detailed Design Procedure

Initial power up:
DC_IN = 0 V; USB = 0 V; EN = 0 V
BAT is applied at 4.2 V
LDO power comes from BAT
LOUT = 3.6 V; CAP = 4.2 V; VOUT = 0 V

USB power is connected at 5 V, BAT remains 4.2 V and DC_IN remains 0 V
LDO power is changed from BAT to USB in t_{CO}

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

DC_IN power is connected at 5.0 V, BAT remains 4.2 V and USB remains 5 V
No change in LDO power

LOUT = 3.6 V; CAP = 5 V; VOUT = 0 V

EN = VIH, BAT remains 4.2 V, USB remains 5 V and DC_IN remains 5 V
LOUT = 3.6 V, CAP = 5 V; VOUT = 3.6 V

USB power is removed, BAT remains 4.2 V and DC_IN remains 5 V
LDO power is changed from USB to DC_IN

LOUT = 3.6 V; CAP = 5 V; VOUT = 3.6 V

DC_IN power is removed, BAT remains 4.2 V and USB remains 0 V:
LDO power is changed from DC_IN to BAT

LOUT = 3.6 V; CAP = 4.2 V; VOUT = 3.6 V

9.2.3 Application Curve

Figure 19 shows the device behavior in the last step of the design procedure, when DC_IN power is removed and the LDO is powered by the battery. The capacitor on the CAP pin discharges as DC_IN is removed but then charges to the battery voltage when the input is automatically switched. LOUT remains a constant 3.6 V throughout this power switching.

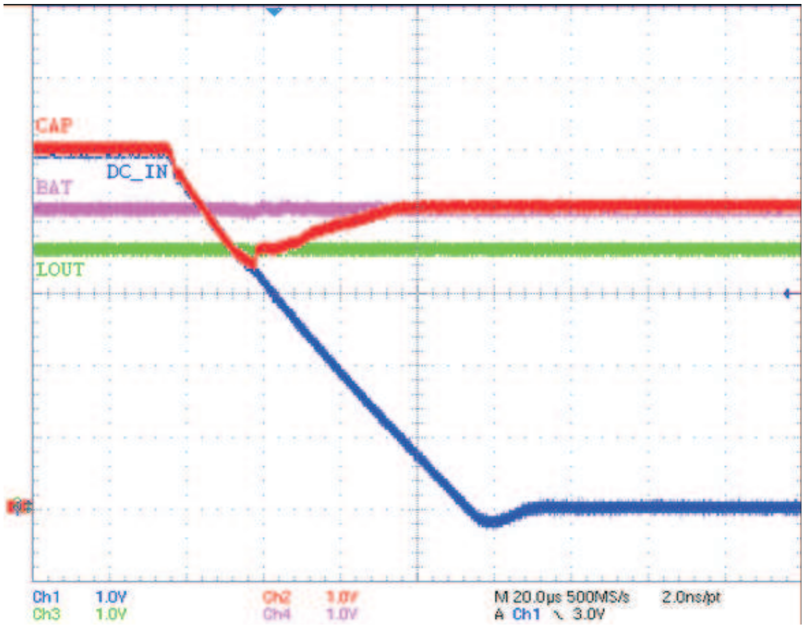


Figure 19. DC_IN Removed, BAT Powers LDO (LOUT = 3.6 V)

10 Power Supply Recommendations

The device is designed to operate with an input voltage range of 2.5 V to 12 V. This supply must be well regulated and placed as close to the device terminals as possible.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short-circuit operation. Using wide traces for BAT, USB, DC_IN, LOUT, VOUT, and GND will help minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

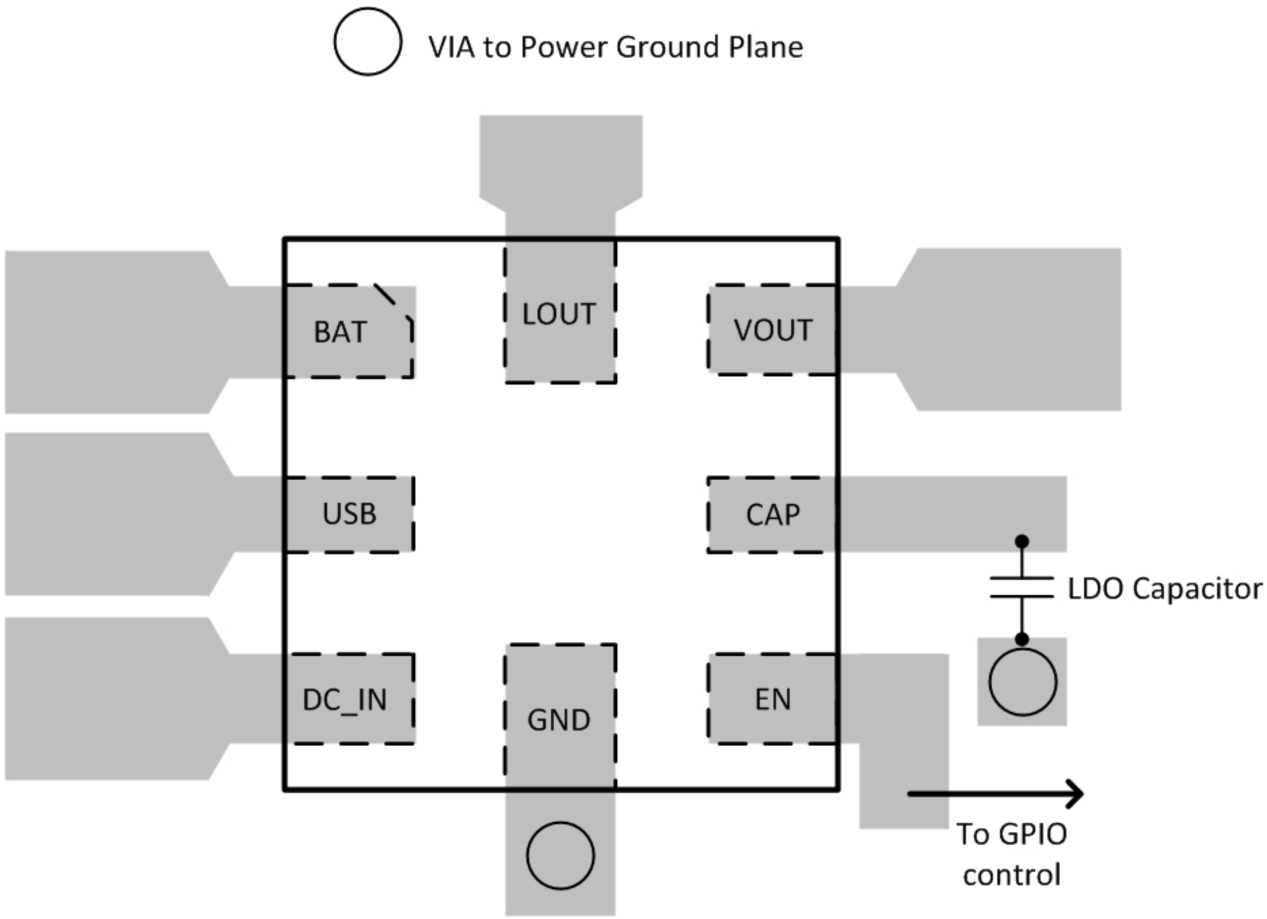


Figure 20. TPS22933 Layout Example

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22933ARSER	ACTIVE	UQFN	RSE	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q	Samples
TPS22933ARSET	ACTIVE	UQFN	RSE	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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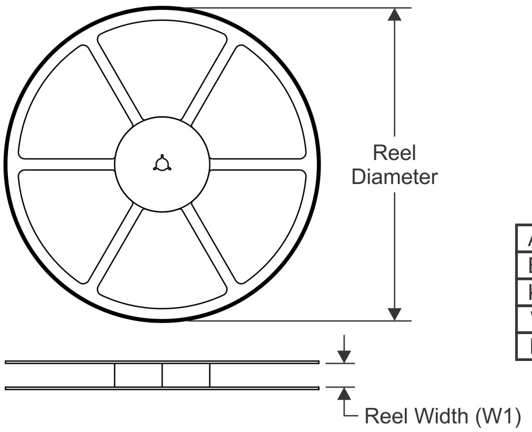
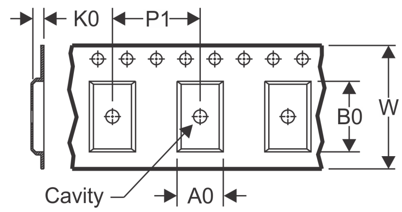
TAPE AND REEL INFORMATION

REEL DIMENSIONS

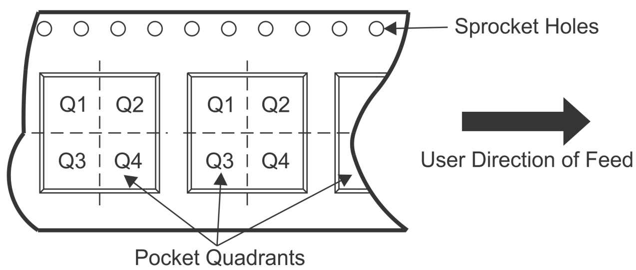


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

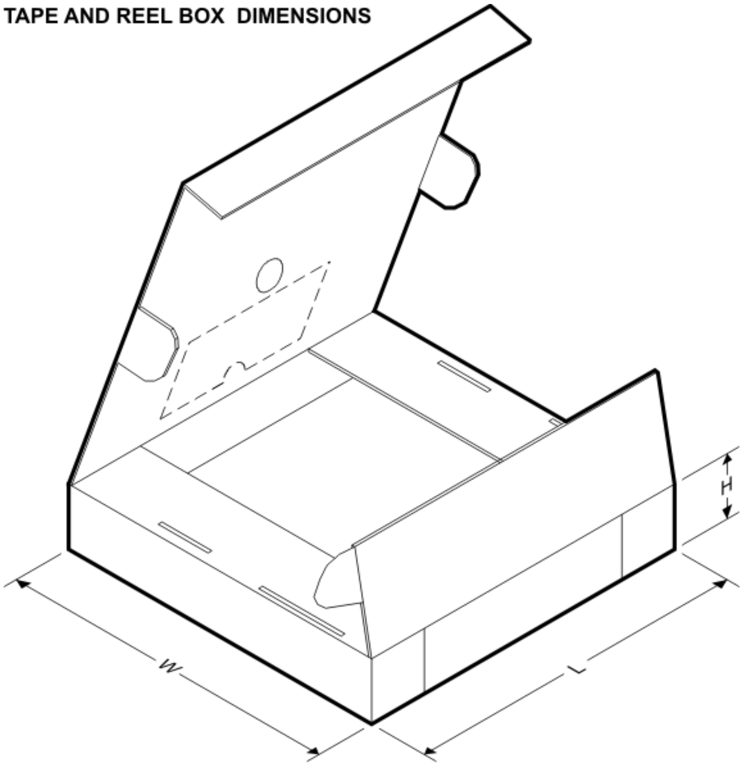
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

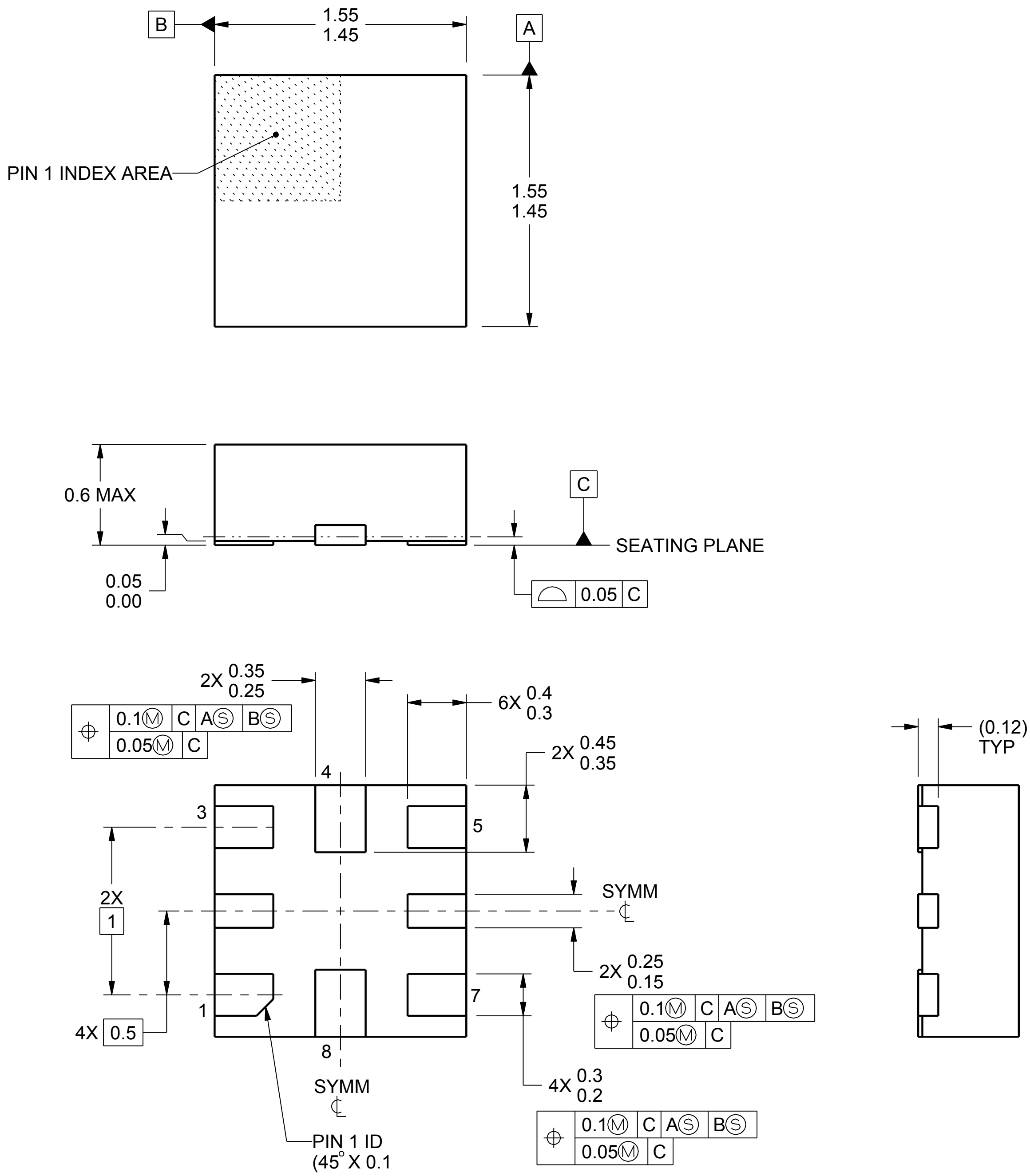
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22933ARSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2
TPS22933ARSET	UQFN	RSE	8	250	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

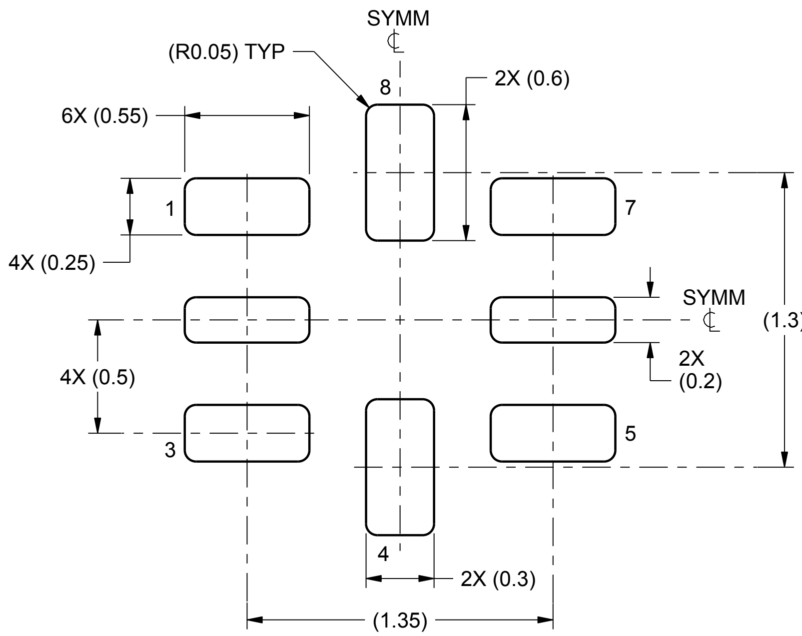
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22933ARSER	UQFN	RSE	8	3000	202.0	201.0	28.0
TPS22933ARSET	UQFN	RSE	8	250	202.0	201.0	28.0



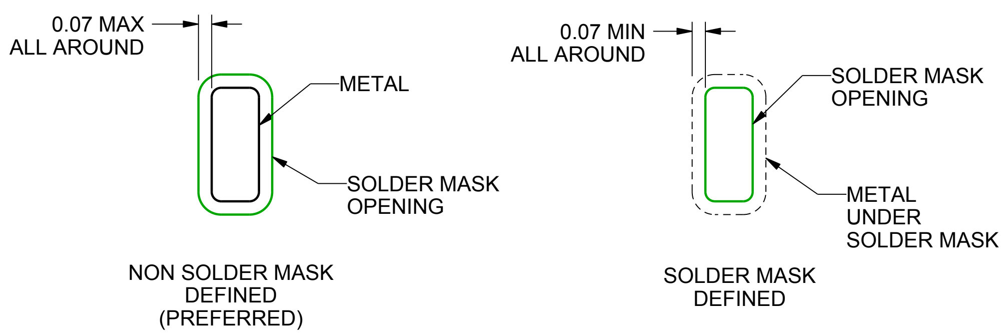
4220323/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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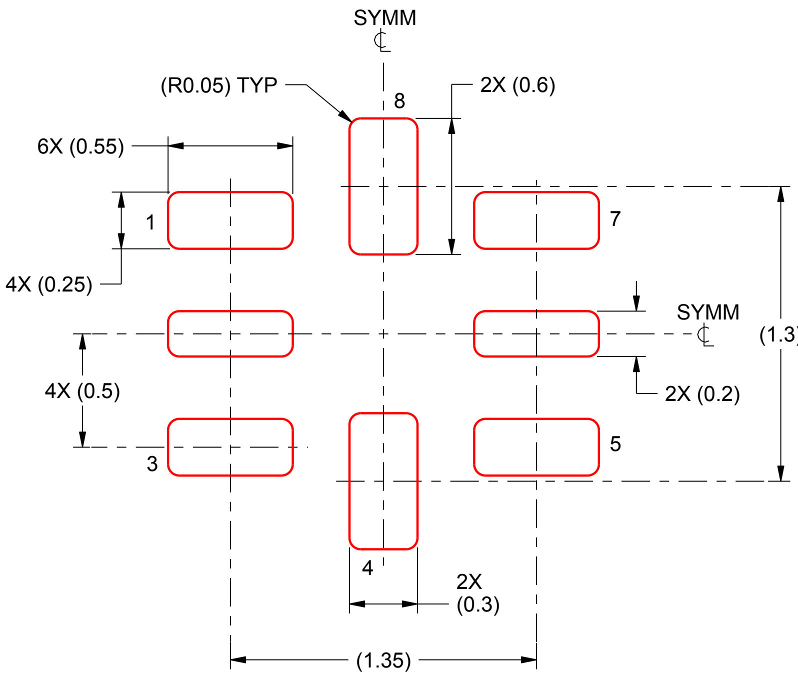
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220323/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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