SN74AUP1G79 Low-Power Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption: I_{CC} = 0.9 μA Max
- Low Dynamic-Power Consumption: C_{pd} = 3 pF Typ at 3.3 V
- Low Input Capacitance: C_i = 1.5 pF Typ
- Low Noise: Overshoot and Undershoot < 10% of V_{CC}
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typ at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4 ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Barcode Scanner
- Cable Solutions
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card

3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, thus resulting in an increased battery life. The AUP devices also maintain excellent signal integrity.

The SN74AUP1G79 is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup-time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

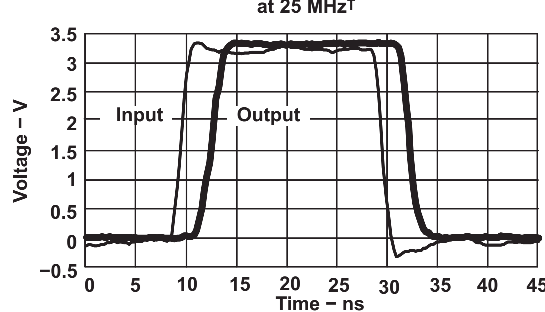
The SN74AUP1G79 device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G79	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SOT (5)	1.60 mm × 1.20 mm
	SON (6)	1.45 mm × 1.00 mm
	SON (6)	1.00 mm × 1.00 mm
	DSBGA (6)	1.16 mm × 0.76 mm
	DSBGA (5)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Power Consumption and Performance



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5 Revision History

Changes from Revision G (May 2010) to Revision H — **Page**

- Updated document to the new TI data sheet format ... 1
- Removed *Ordering Information* table ... 1
- Added DPW Package ... 3
- Added *Typical Characteristics* section ... 10

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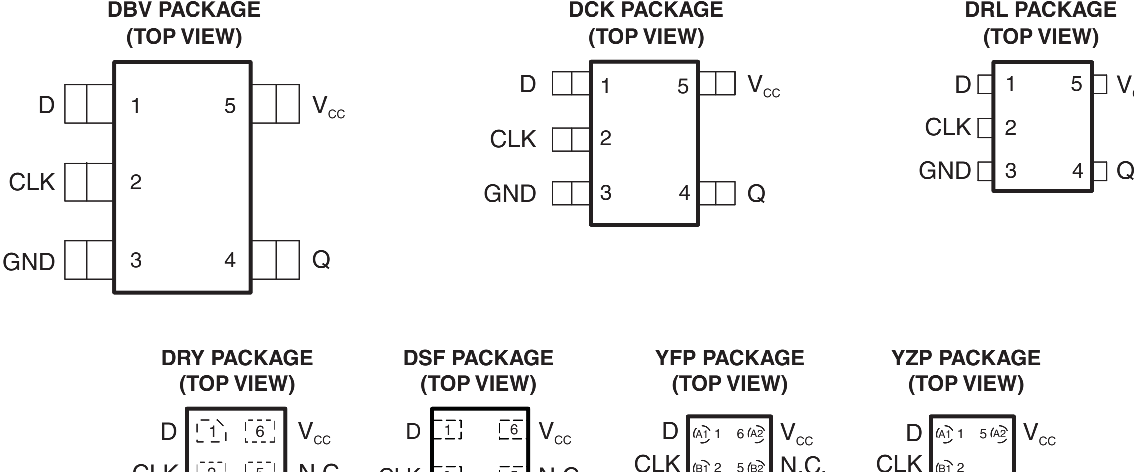
6 Pin Configuration and Functions



Pin Functions

PIN					I/O	DESCRIPTION
NAME	DBV, DCK, DRL	DRY, DSF	YZP	YFP		
CLK	2	2	B1	B1	I	Clock Input
D	1	1	A1	A1	I	Data Input
GND	3	3	C1	C1	—	Ground
N.C.	—	5	—	B2	—	No Connect
Q	4	4	C2	C2	O	Q Output
V_{CC}	5	6	A2	A2	—	Power

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	4.6	V
V_O	Output voltage range in the high or low state[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	+2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	+1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage (1)		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	µA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.4 Thermal Information

THERMAL METRIC (1)		SN74AUP1G79							UNIT
		DBV	DCK	DRL	DRY	DSF	YFP	YZP	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	142	234	300	132	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –20 μA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	D or CLK input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}		V_I = GND or V_{CC} to 3.6 V, I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		V_I = V_{CC} – 0.6 V,(1) I_O = 0	3.3 V			40		50	μA
C_i		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = GND	0 V		3				pF

(1) One-input switching

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7.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V_{CC}	T_A = 25°C	T_A = –40°C to 85°C		UNIT
				TYP	MIN	MAX	
f_{clock}	Clock frequency		0.8 V			20	MHz
			1.2 V ± 0.1 V			80	
			1.5 V ± 0.1 V			100	
			1.8 V ± 0.15 V			140	
			2.5 V ± 0.2 V			210	
			3.3 V ± 0.3 V			260	
t_w	Pulse duration, CLK high or low		0.8 V		4.8		ns
			1.2 V ± 0.1 V		2.2		
			1.5 V ± 0.1 V		1.5		
			1.8 V ± 0.15 V		1.6		
			2.5 V ± 0.2 V		1.7		
			3.3 V ± 0.3 V		1.9		
t_{su}	Setup time before CLK↑	Data high	0.8 V	2.9	4.2		ns
			1.2 V ± 0.1 V		1.4		
			1.5 V ± 0.1 V		1		
			1.8 V ± 0.15 V		0.9		
			2.5 V ± 0.2 V		0.7		
			3.3 V ± 0.3 V		0.6		
		Data low	0.8 V	3.5	5.3		
			1.2 V ± 0.1 V		1.8		
			1.5 V ± 0.1 V		1.2		
			1.8 V ± 0.15 V		1.1		
			2.5 V ± 0.2 V		1		
			3.3 V ± 0.3 V		1		
t_h	Hold time, data after CLK↑		0.8 V	0	0		ns
			1.2 V ± 0.1 V		0		
			1.5 V ± 0.1 V		0		
			1.8 V ± 0.15 V		0		
			2.5 V ± 0.2 V		0		
			3.3 V ± 0.3 V		0		

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7.7 Switching Characteristics

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to 85°C MIN	T_A = –40°C to 85°C MAX	UNIT
f_{max}			0.8 V		93		90		MHz
			1.2 V ± 0.1 V		199		220		
			1.5 V ± 0.1 V		250		230		
			1.8 V ± 0.15 V		271		240		
			2.5 V ± 0.2 V		280		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		15.9				ns
			1.2 V ± 0.1 V	3.7	6.9	11	2.6	13.1	
			1.5 V ± 0.1 V	3	4.8	7.6	2	8.8	
			1.8 V ± 0.15 V	2.4	3.8	6.1	1.5	7.1	
			2.5 V ± 0.2 V	1.8	2.7	4.4	1.1	5	
			3.3 V ± 0.3 V	1.5	2.1	3.6	0.9	4	

7.8 Switching Characteristics

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	T_A = –40°C to 85°C MIN	T_A = –40°C to 85°C MAX	UNIT
f_{max}			0.8 V		62		50		MHz
			1.2 V ± 0.1 V		147		160		
			1.5 V ± 0.1 V		189		200		
			1.8 V ± 0.15 V		180		240		
			2.5 V ± 0.2 V		260		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		18				ns
			1.2 V ± 0.1 V	4.3	7.8	12.3	3.2	14.4	
			1.5 V ± 0.1 V	3.5	5.5	8.4	2.5	9.8	
			1.8 V ± 0.15 V	2.8	4.4	6.8	1.9	8	
			2.5 V ± 0.2 V	2.2	3.2	5	1.5	5.7	
			3.3 V ± 0.3 V	1.8	2.6	4.1	1.3	4.5	

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7.9 Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		48		30		MHz
			1.2 V ± 0.1 V		112		120		
			1.5 V ± 0.1 V		151		160		
			1.8 V ± 0.15 V		194		220		
			2.5 V ± 0.2 V		248		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	Q	0.8 V		20.3				ns
			1.2 V ± 0.1 V	5	8.7	13.6	3.9	15.6	
			1.5 V ± 0.1 V	4.1	6.3	9.3	3.1	10.7	
			1.8 V ± 0.15 V	3.3	4	7.6	2.4	8.7	
			2.5 V ± 0.2 V	2.6	3.6	5.5	1.9	6.3	
			3.3 V ± 0.3 V	2.2	3	4.5	1.6	5	

7.10 Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		24		20		MHz
			1.2 V ± 0.1 V		72		80		
			1.5 V ± 0.1 V		100		100		
			1.8 V ± 0.15 V		127		140		
			2.5 V ± 0.2 V		185		210		
			3.3 V ± 0.3 V		266		260		
t_{pd}	CLK	Q	0.8 V		27.2				ns
			1.2 V ± 0.1 V	7	11.5	17.3	5.9	24	
			1.5 V ± 0.1 V	5.7	8.3	11.8	4.6	15.9	
			1.8 V ± 0.15 V	4.7	6.7	9.6	3.8	13	
			2.5 V ± 0.2 V	3.7	4.9	7	2.9	9	
			3.3 V ± 0.3 V	3.2	4.1	5.8	2.6	7.2	

7.11 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	2.5	pF
			1.2 V ± 0.1 V	2.5	
			1.5 V ± 0.1 V	2.5	
			1.8 V ± 0.15 V	2.5	
			2.5 V ± 0.2 V	3	
			3.3 V ± 0.3 V	3	

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7.12 Typical Characteristics

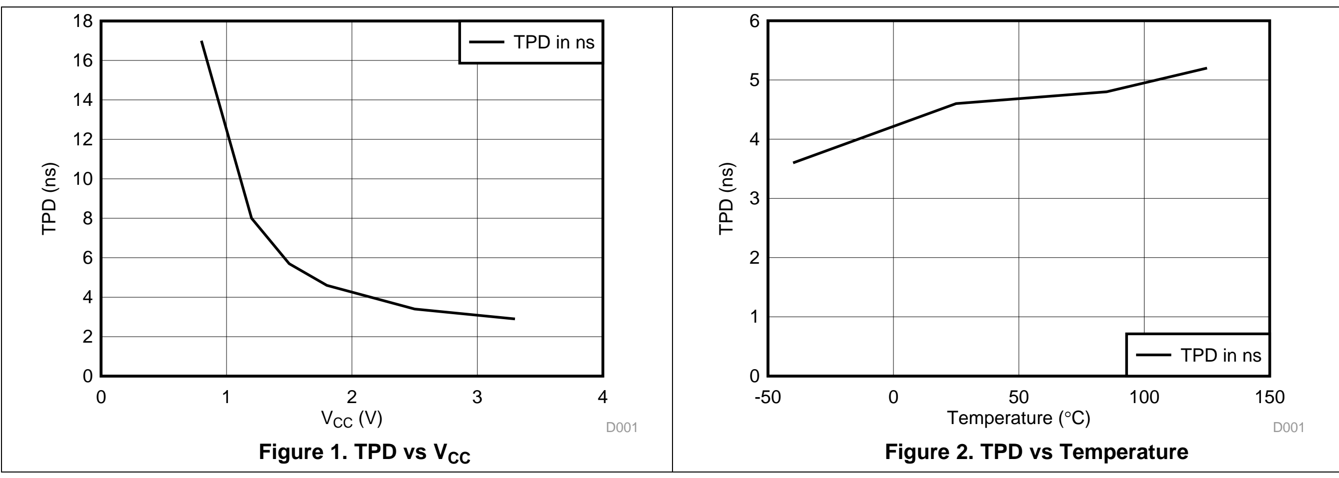

Figure 1. TPD vs V_{CC}

Figure 2. TPD vs Temperature

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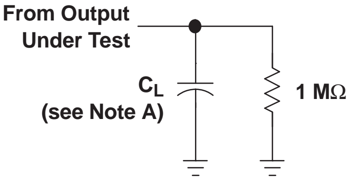
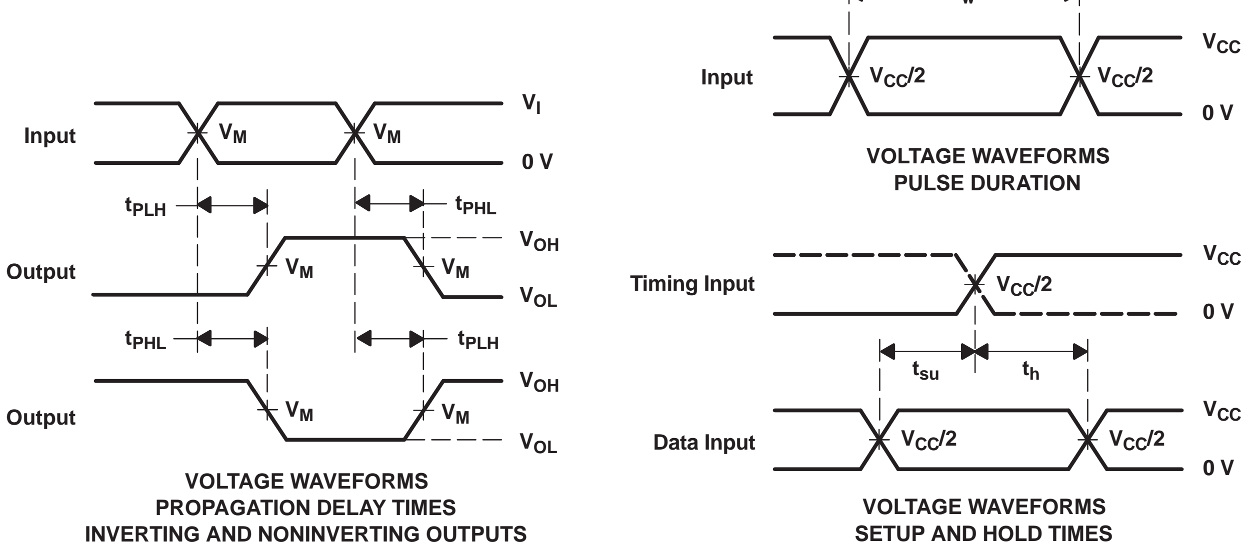
8 Parameter Measurement Information (Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



NOTES:
A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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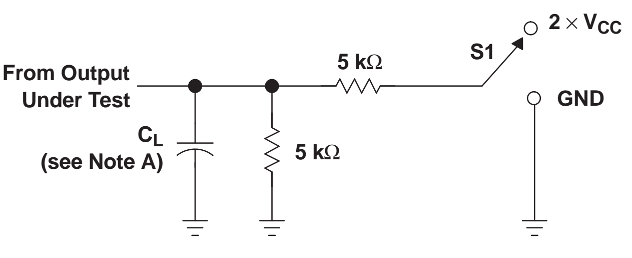
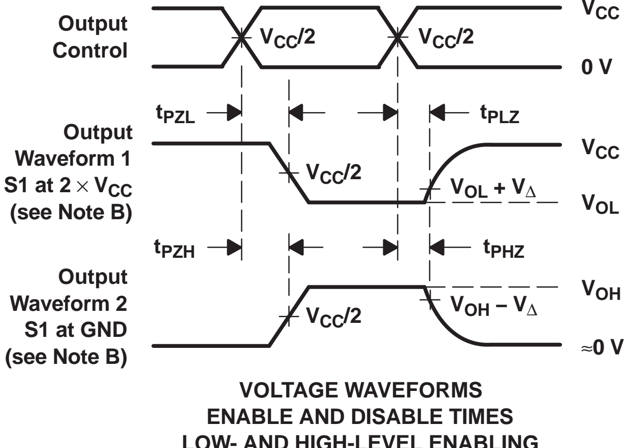
9 Parameter Measurement Information

(Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

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10 Detailed Description

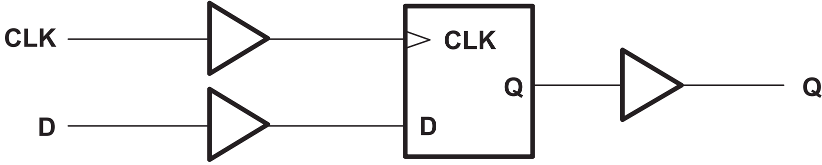
10.1 Overview

The SN74AUP1G79 device is a single positive-edge-triggered D-Type flip-flop that is designed using Texas Instruments' ultra-low power technology.

The AUP family of devices has quiescent power consumption of less than 1 µA.

The SN74AUP1G79 device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs and prevents damaging current backflow through the device when it is powered. The I_{off} feature also allows for live insertion.

10.2 Functional Block Diagram



10.3 Feature Description

The SN74AUP1G79 device has a wide operating V_{CC} range of 0.8 V to 3.6 V, which allows it to be used in multiple types of systems. The 3.6-V I/Os allow down translation and also allow voltages at the inputs when V_{CC} = 0. Input hysteresis allows slow input transition and better switching noise immunity at the input.

10.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Q
CLK	D	
↑	H	H
↑	L	L
L or H	X	Q_0

11 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. The AUP family ensures a very low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, thus resulting in an increased battery life. The SN74AUP1G79 device also maintains excellent signal integrity. It has a small amount of hysteresis built in, which allows for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

11.2 Typical Application

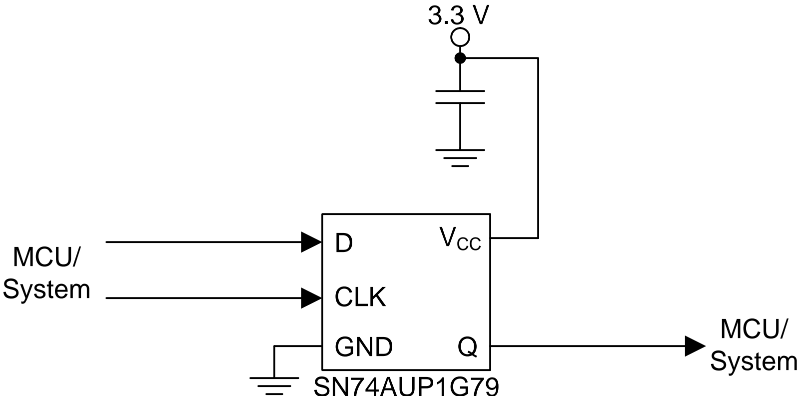


Figure 5. Typical Application Diagram

11.2.1 Design Requirements

The SN74AUP1G79 device uses CMOS technology and has balanced output drive. Care must be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

11.2.2 Detailed Design Procedure

1. Recommended Input conditions
   – Rise time and fall time specifications. See Δt/ΔV in *Recommended Operating Conditions* .
   – Specified high and low levels. See V_{IH} and V_{IL} in *Recommended Operating Conditions* .
   – Inputs are overvoltage tolerant, which allows them to go as high as 3.6 V at any valid V_{CC}
2. Recommend output conditions
   – Load currents must not exceed 20 mA on the output and 50 mA total for the part
   – Outputs must not be pulled above V_{CC}

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Typical Application (continued)

11.2.3 Application Curves

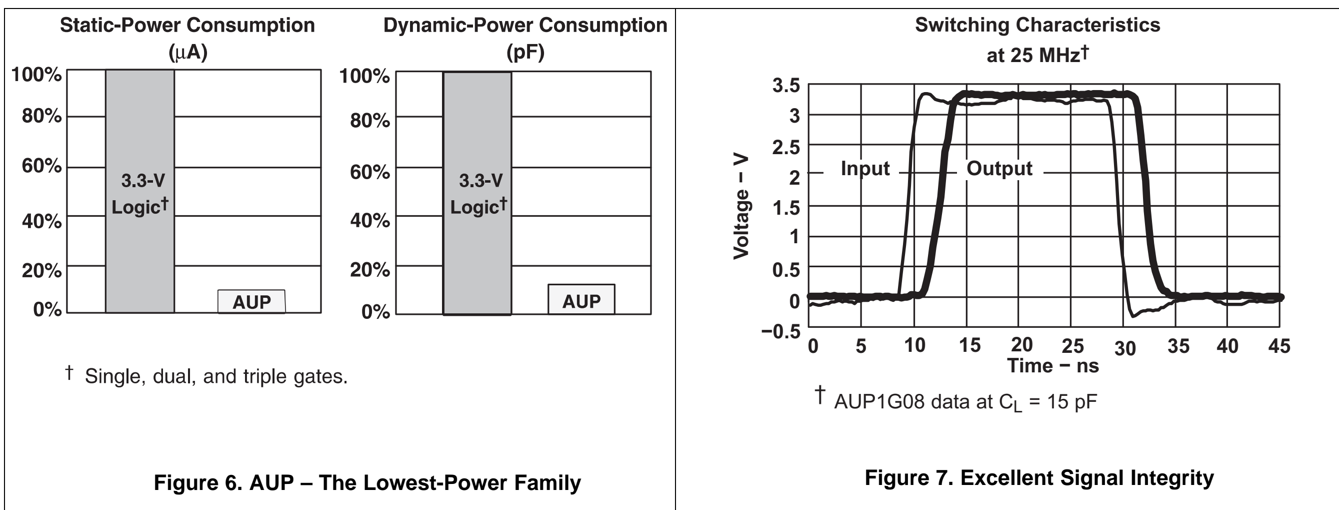

Figure 6. AUP – The Lowest-Power Family

Figure 7. Excellent Signal Integrity

The single-gate logic AUP family devices make excellent translators for the new lower-voltage microprocessors, which are typically powered from 0.8 V to 1.2 V. The AUP devices can translate the voltage of peripheral drivers and accessories still powered by 3.3 V to the new µC power levels.

12 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 µF is recommended; if there are multiple V_{CC} pins, then 0.01 µF or 0.022 µF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 µF and a 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

13 Layout

13.1 Layout Guidelines

When using multiple-bit logic devices, inputs must never float.

In many cases, functions (or parts of functions) of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or when only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected, because the undefined voltages at the outside connections result in undefined operational states. Figure 8 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted, which does not disable the input section of the I/Os. Therefore, the I/Os cannot float when disabled.

13.2 Layout Example

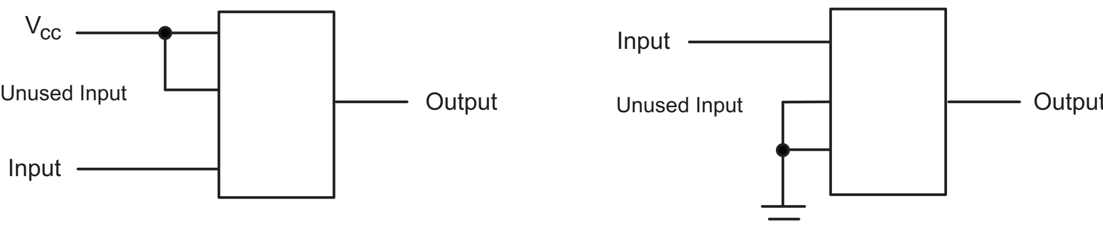

Figure 8. Layout Diagram

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14 Device and Documentation Support

14.1 Trademarks

NanoStar is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

14.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

14.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G79DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HWF ~ HWK ~ HWO ~ HWR)	Samples
SN74AUP1G79DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HWO ~ HWR)	Samples
SN74AUP1G79DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HWO ~ HWR)	Samples
SN74AUP1G79DRLR	ACTIVE	SOT-OTHER	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HWR	Samples
SN74AUP1G79DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HW	Samples
SN74AUP1G79DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HW	Samples
SN74AUP1G79YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		HWN	Samples
SN74AUP1G79YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HWN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

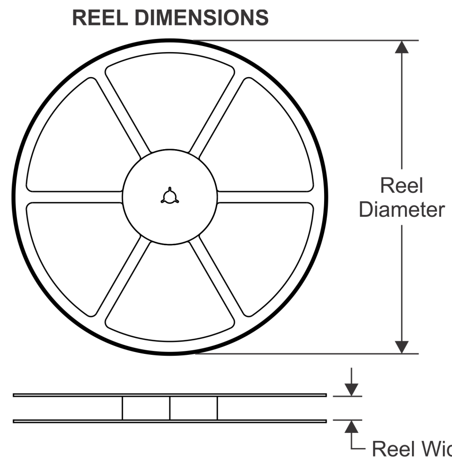
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

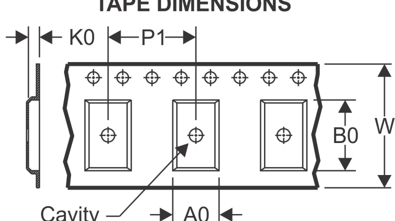
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

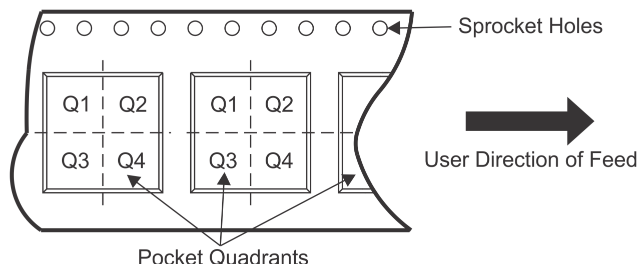
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

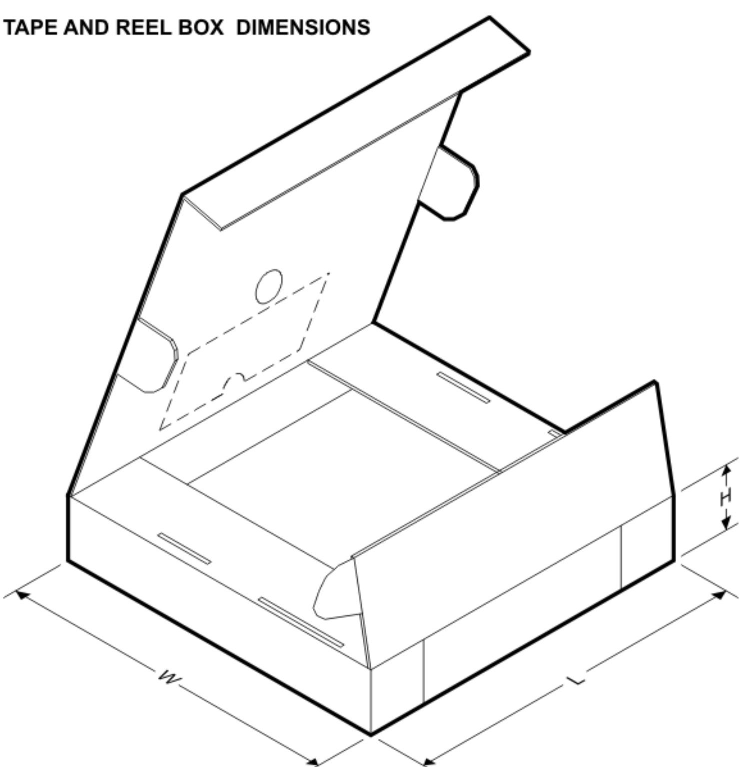
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G79DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G79DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G79DRLR	SOT-OTHER	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G79DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G79DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G79YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G79DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G79DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G79DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G79DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G79DRLR	SOT-OTHER	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G79DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G79DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G79YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

1,50
1,40
A
B
6 5 4
1,05
0,95
1 2 3
Pin 1 Index Area

0,60
0,51
// 0,05 C
0,15 Nominal
Lead Frame
D
Seating Plane
0,05 C
0,05
0,00
Seating Height
C

1,00
0,50
1 2 3
6X 0,10 / 0,00
F Pin 1 Identifier
Pin shape will be
modified per device.
5X 0,45 / 0,25
5X 0,35 / 0,25
6 5 4
6X 0,25 / 0,15
0,10 (M) C A B
0,05 (M) C

Bottom View

4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

Example Board Layout

Example Stencil Design
(Note E, F, G)

1
0,5
1,26
0,25
0,52
0,49
0,26
0,3

Example Solder Mask Clearance
(Note D)

Example Pad Geometry
(Note C)

0,05
0,1
0,05
0,05
0,05

4208310/E 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

B E A

BALL A1 CORNER

D

0.5 MAX

C

SEATING PLANE

0.19
0.13

BALL TYP

0.05 C

0.4 TYP

SYMM

C

B

A

0.8 TYP

0.4 TYP

SYMM

6X ∅ 0.25
0.21

0.015 Ⓜ C A B

1 2

D: Max = 1.19 mm, Min = 1.13 mm

E: Max = 0.79 mm, Min = 0.73 mm

4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

(0.4) TYP
6X (∅0.23)
1 2
A
B
C
(0.4) TYP
SYMM ℄
SYMM ℄

LAND PATTERN EXAMPLE
SCALE:50X

(∅0.23) METAL
0.05 MAX
SOLDER MASK OPENING
NON-SOLDER MASK DEFINED (PREFERRED)

0.05 MIN
METAL UNDER SOLDER MASK
(∅0.23) SOLDER MASK OPENING
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

(0.4) TYP
6X (□0.25)
(R0.05) TYP
1
2
A
(0.4) TYP
B
SYMM
℄
METAL
TYP
C
SYMM
℄

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout

1,00
0,45
1,80
0,90
0,30
0,50

Example
Non–Soldermask Defined Pad

Example
Pad Geometry

0,05
All Around

Example
Non–Soldermask Opening

Example Stencil Design
(Note E)

1,00
0,55
1,90
0,80
0,40
0,50

4208207–2/E 06/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90
1,90
1,00
0,55
2,7
2,7
0,95
0,95
0,6
Solder Mask Opening
1,05
Pad Geometry
0,07
All Around

4209593-3/C 08/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DSF (S-PX2SON-N6) PLASTIC SMALL OUTLINE NO-LEAD

A 1.05 0.95 B

PIN 1 INDEX AREA

1.05 0.95

0.4 MAX

C

SEATING PLANE

0.05Ⓜ C

(0.11) TYP

0.05 0.00

SYMM

3

4

2X 0.7

4X 0.35

SYMM

6

1

6X 0.22 0.12

(0.1) PIN 1 ID

6X 0.45 0.35

0.07Ⓜ C AⓈ BⓈ

0.05Ⓜ C

4208186/F 10/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

DSF (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

2,15
1,85
5
4
2,40
1,80
1,40
1,10
Pin 1
Index Area
1
3
0,65
5X 0,30
0,15
0,10 Ⓜ
1,30

0,22
0,08
Gauge Plane
Seating Plane
0,15
0°–8°
0,46
0,26

1,10
0,80
0,10
Seating Plane
0,10
0,00

4093553-3/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35
0,85
2,2
2,2
2x0,65
2x1,30
2x0,65
2x1,30
0,4
Solder Mask Opening
1,0
0,9
Pad Geometry
0,05
0,50

4210356–2/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY

D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

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NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

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